查询TEA1506供应商

DATA SHEET

TEA1506P; TEA1506AP; TEA1506T; TEA1506AT

GreenChip™II SMPS control IC

Product specification

2003 Sep 09

Philips Semiconductors

PHILIPS

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TEA1506P; TEA1506AP; TEA1506T; TEA1506AT

FEATURES

Distinctive features

- Universal mains supply operation (70 to 276 V AC)
- High level of integration; giving a low external component count.

Green features

- Valley or zero voltage switching for minimum switching losses
- Efficient quasi-resonant operation at high power levels
- Frequency reduction at low power standby for improved system efficiency (≤3 W)
- Cycle skipping mode at very low loads.

Protection features

- Safe restart mode for system fault conditions
- Continuous mode protection by means of demagnetization detection (zero switch-on current)
- Accurate and adjustable overvoltage protection (latched in TEA1506; safe restart in TEA1506A)
- Short winding protection
- Undervoltage protection (foldback during overload)
- Overtemperature protection
- Low and adjustable overcurrent protection trip level
- Soft (re)start.

APPLICATIONS

Besides typical application areas, i.e. TV and monitor supplies, the device can be used in adapters and chargers and all applications that demand an efficient and cost-effective solution up to 150 W. Unlike the other GreenChip™II control ICs, the TEA1506 has no internal high voltage start-up source and needs to be started by means of an external bleeder resistor.

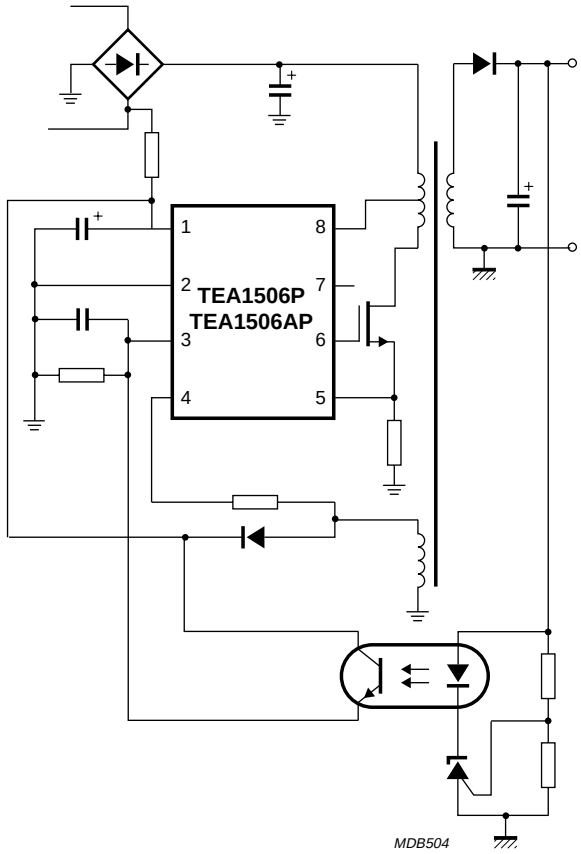


Fig.1 Basic application diagram.

GENERAL DESCRIPTION

The GreenChip™(1)II is the second generation of green Switched Mode Power Supply (SMPS) control ICs. A high level of integration leads to a cost effective power supply with a low number of external components.

(1) GreenChip is a trademark of Koninklijke Philips Electronics N.V.

The special built-in green functions allow the efficiency to be optimum at all power levels. This holds for quasi-resonant operation at high power levels, as well as fixed frequency operation with valley switching at medium power levels. At low power (standby) levels, the system operates at a reduced frequency and with valley detection.

Highly efficient and reliable supplies can easily be designed using the GreenChip™II control IC.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1506P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TEA1506AP			
TEA1506T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TEA1506AT			

BLOCK DIAGRAM

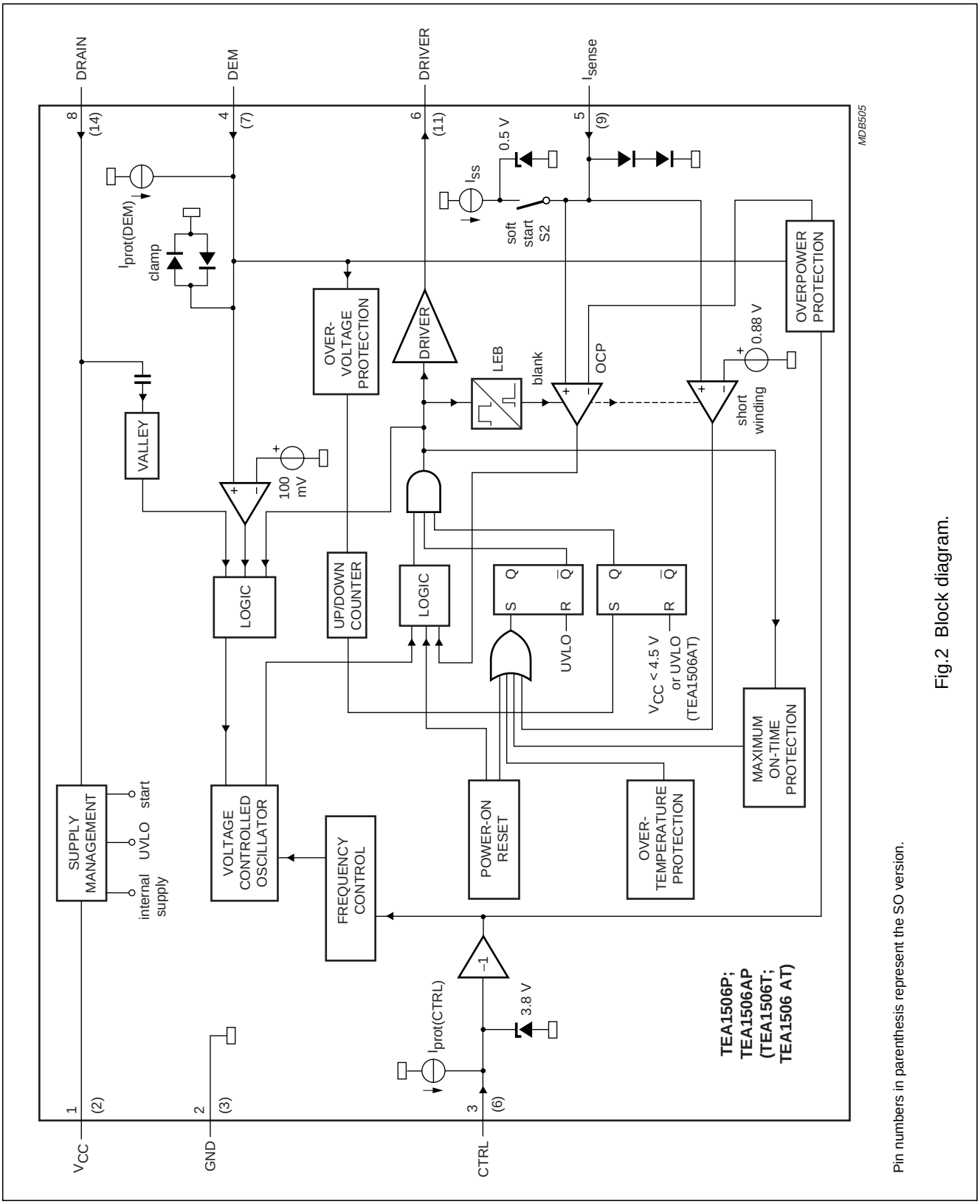


Fig.2 Block diagram.

Pin numbers in parenthesis represent the SO version.

PINNING

SYMBOL	PIN		DESCRIPTION
	DIP8	SO14	
V_{CC}	1	2	supply voltage
GND	2	3	ground
CTRL	3	6	control input
DEM	4	7	input from auxiliary winding for demagnetization timing; overvoltage and overpower protection
I_{sense}	5	9	programmable current sense input
DRIVER	6	11	gate driver output
HVS	7	12, 13	high voltage safety spacer; not connected
DRAIN	8	14	drain of external MOS switch; input for valley sensing and initial internal supply
n.c.	–	1, 4, 5, 8, 10	not connected

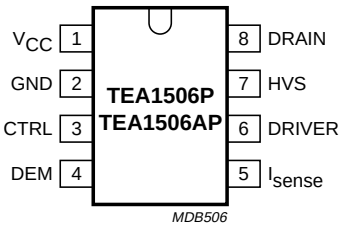


Fig.3 Pin configuration DIP8.

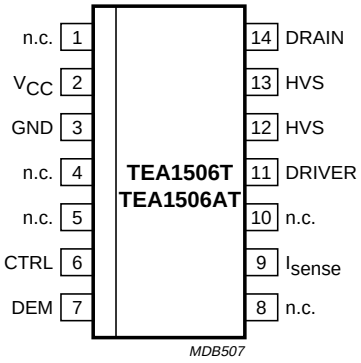


Fig.4 Pin configuration SO14.

FUNCTIONAL DESCRIPTION

The TEA1506 is the controller of a compact flyback converter, and is situated at the primary side. An auxiliary winding of the transformer provides demagnetization detection and powers the IC after start-up.

The TEA1506 can operate in multi modes (see Fig.5).

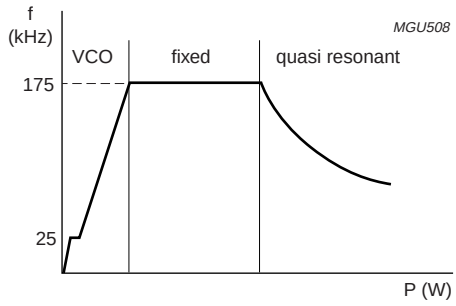


Fig.5 Multi modes operation.

The next converter stroke is started only after demagnetization of the transformer current (zero current switching), while the drain voltage has reached the lowest voltage to prevent switching losses (green function). The primary resonant circuit of the primary inductance and drain capacitor ensures this quasi-resonant operation. The design can be optimized in such a way that zero voltage switching can be reached over almost the universal mains range.

To prevent very high frequency operation at lower loads, the quasi-resonant operation changes smoothly in fixed frequency PWM control.

At very low power (standby) levels, the frequency is controlled down, via the VCO, to a minimum frequency of approximately 25 kHz.

Start-up and undervoltage lock-out

Initially the IC is in the save restart mode. As long as V_{CC} is below the $V_{CC(start)}$ level, the supply current is nearly zero.

The IC will activate the converter as soon as the voltage on pin V_{CC} passes the $V_{CC(start)}$ level.

The IC supply is taken over by the auxiliary winding as soon as the output voltage reaches its intended level.

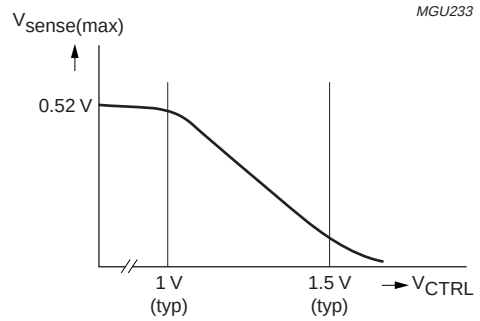


Fig.6 $V_{sense(max)}$ voltage as function of V_{CTRL}.

The moment the voltage on pin V_{CC} drops below the undervoltage lock-out level, the IC stops switching and re-enters the safe restart mode.

Supply management

All (internal) reference voltages are derived from a temperature compensated, on-chip band gap circuit.

Current mode control

Current mode control is used for its good line regulation behaviour.

The ‘on-time’ is controlled by the internally inverted control voltage, which is compared with the primary current information. The primary current is sensed across an external resistor. The driver output is latched in the logic, preventing multiple switch-on.

The internal control voltage is inversely proportional to the external control pin voltage, with an offset of 1.5 V. This means that a voltage range from 1 to 1.5 V on pin CTRL will result in an internal control voltage range from 0.5 to 0 V (a high external control voltage results in a low duty cycle).

Oscillator

The maximum fixed frequency of the oscillator is set by an internal current source and capacitor. The maximum frequency is reduced once the control voltage enters the VCO control window. Then, the maximum frequency changes linearly with the control voltage until the minimum frequency is reached (see Figs 6 and 7).

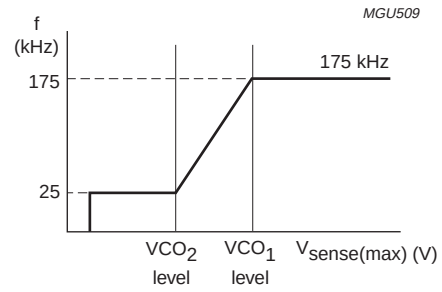


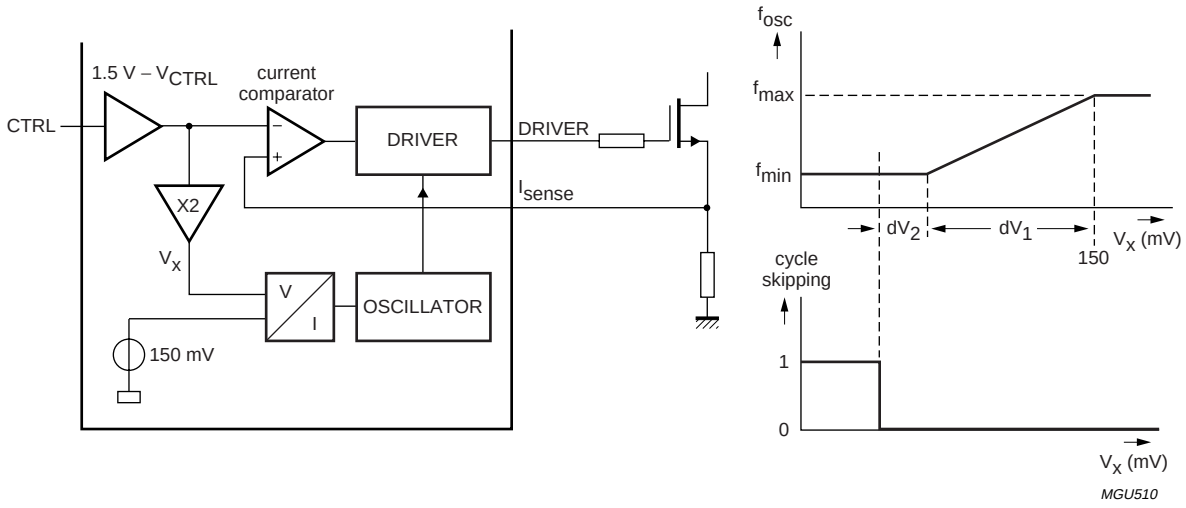
Fig.7 VCO frequency as function of $V_{sense(max)}$.

Cycle skipping

At very low power levels, a cycle skipping mode will be activated. A high control voltage will reduce the switching frequency to a minimum of 25 kHz. If the voltage on the control pin is raised even more, switch-on of the external power MOSFET will be inhibited until the voltage on the control pin has dropped to a lower value again (see Fig.8).

For system accuracy, it is not the absolute voltage on the control pin that will trigger the cycle skipping mode, but a signal derived from the internal VCO will be used.

Remark: If the no-load requirement of the system is such that the output voltage can be regulated to its intended level at a switching frequency of 25 kHz or above, the cycle skipping mode will not be activated.



The voltage levels dV_1 and dV_2 are fixed in the IC to 50 mV (typical) and 18 mV (typical) respectively.

Fig.8 The cycle skipping circuitry.

Demagnetization

The system will be in discontinuous conduction mode all the time. The oscillator will not start a new primary stroke until the secondary stroke has ended.

Demagnetization features a cycle-by-cycle output short-circuit protection by immediately lowering the frequency (longer off-time), thereby reducing the power level.

Demagnetization recognition is suppressed during the first t_{suppr} time. This suppression may be necessary in applications where the transformer has a large leakage inductance, at low output voltages and at start-up.

If pin DEM is open-circuit or not connected, a fault condition is assumed and the converter will stop operating immediately. Operation will recommence as soon as the fault condition is removed.

Minimum and maximum 'on-time'

The minimum 'on-time' of the SMPS is determined by the Leading Edge Blanking (LEB) time. The IC limits the 'on-time' to 50 μs. When the system desires an 'on-time' longer than 50 μs, a fault condition is assumed (e.g. removed C_i in Fig.12), the IC will stop switching and enter the safe restart mode.

OverVoltage Protection (OVP)

An OVP mode is implemented in the GreenChip series. This works for the TEA1506 by sensing the auxiliary voltage via the current flowing into pin DEM during the secondary stroke. The auxiliary winding voltage is a well-defined replica of the output voltage. Any voltage spikes are averaged by an internal filter.

If the output voltage exceeds the OVP trip level, an internal counter starts counting subsequent OVP events. The counter has been added to prevent incorrect OVP detections which might occur during ESD or lightning events. If the output voltage exceeds the OVP trip level a few times and not again in a subsequent cycle, the internal counter will count down with twice the speed compared with counting-up. However, when typical 10 cycles of subsequent OVP events are detected, the IC assumes a true OVP and the OVP circuit switches the power MOSFET off. Next, the controller waits until the UVLO level is reached on pin V_{CC}. When V_{CC} drops to UVLO, capacitor C_{VCC} will be recharged to the V_{start} level.

Regarding the TEA1506, the IC will not start switching again. Subsequently, V_{CC} will drop again to the UVLO level, etc.
Operation only recommences when the V_{CC} voltage drops below a level of about 4.5 V.

Regarding the TEA1506A, when the V_{start} level is reached, switching starts again (safe restart mode) when the V_{start} level is reached. This process is repeated as long as the OVP condition exists.

The output voltage $V_{o(OVP)}$ at which the OVP function trips, can be set by the demagnetization resistor, R_{DEM}:

$$V_{o(OVP)} = \frac{N_s}{N_{aux}}\{I_{(OVP)(DEM)} \times R_{DEM} + V_{clamp(DEM)(pos)}\}$$

where N_s is the number of secondary turns and N_{aux} is the number of auxiliary turns of the transformer.

Current $I_{(OVP)(DEM)}$ is internally trimmed.

The value of R_{DEM} can be adjusted to the turns ratio of the transformer, thus making an accurate OVP possible.

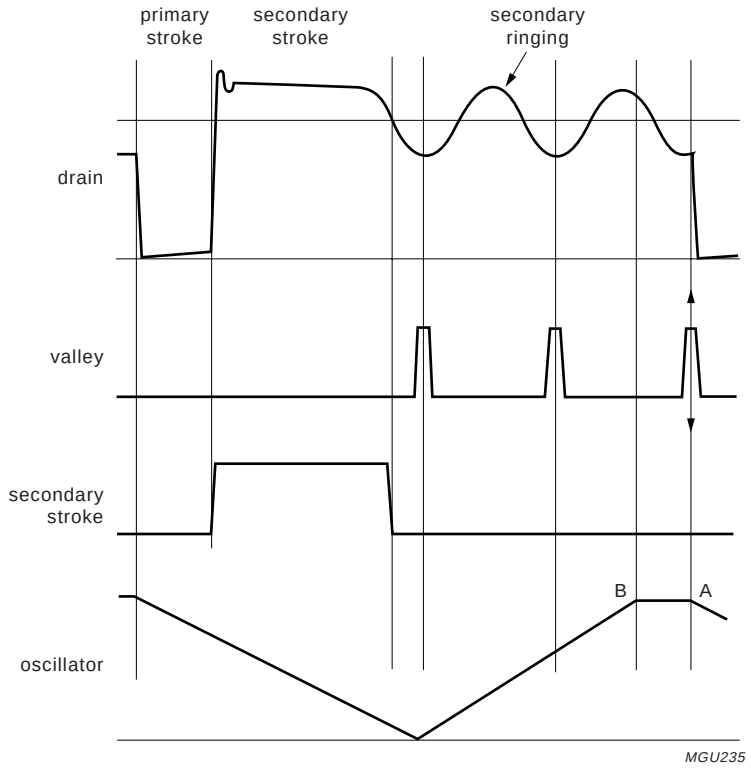
Valley switching

A new cycle starts when the power MOSFET is switched on (see Fig.9). After the 'on-time' (which is determined by the 'sense' voltage and the internal control voltage), the switch is opened and the secondary stroke starts. After the secondary stroke, the drain voltage shows an oscillation with a frequency of approximately $\frac{1}{2 \times \pi \times \sqrt{(L_p \times C_d)}}$

where L_p is the primary self inductance of the transformer and C_d is the capacitance on the drain node.

As soon as the oscillator voltage is high again and the secondary stroke has ended, the circuit waits for the lowest drain voltage before starting a new primary stroke. This method is called valley detection.
Figure 9 shows the drain voltage together with the valley signal, the signal indicating the secondary stroke and the oscillator signal.

In an optimum design, the reflected secondary voltage on the primary side will force the drain voltage to zero. Thus, zero voltage switching is very possible, preventing large capacitive switching losses $\left(P = \frac{1}{2} \times C \times V^2 \times f\right)$ and allowing high frequency operation, which results in small and cost effective inductors.



A: Start of new cycle at lowest drain voltage.
B: Start of new cycle in a classical PWM system at high drain voltage.

Fig.9 Signals for valley switching.

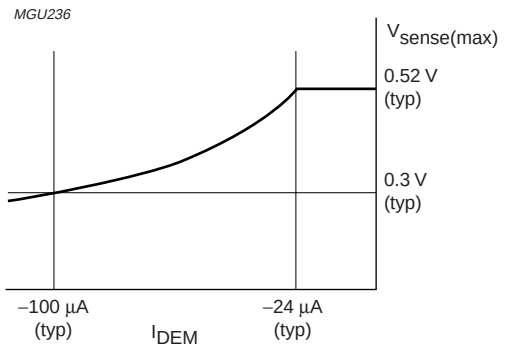


Fig.10 OPP correction curve.

OverCurrent Protection (OCP)

The cycle-by-cycle peak drain current limit circuit uses the external source resistor to measure the current accurately. This allows optimum size determination of the transformer core (cost issue). The circuit is activated after the leading edge blanking time, t_{leb}. The OCP circuit limits the 'sense' voltage to an internal level.

OverPower Protection (OPP)

During the primary stroke, the rectified mains input voltage is measured by sensing the current drawn from pin DEM. This current is dependent on the mains voltage, according to the following formula: $I_{DEM} \approx \frac{V_{aux}}{R_{DEM}} \approx \frac{N \times V_{mains}}{R_{DEM}}$

where: $N = \frac{N_{aux}}{N_p}$

The current information is used to adjust the peak drain current, which is measured via pin I_{sense}. The internal compensation is such that an almost mains independent maximum output power can be realized.

The OPP curve is given in Fig.10.

Short winding protection

After the leading edge blanking time, the short winding protection circuit is activated. If the 'sense' voltage exceeds the short winding protection voltage V_{swp}, the converter will stop switching. Once V_{CC} drops below the UVLO level, capacitor C_{VCC} will be recharged and the supply will restart again. This cycle will be repeated until the short-circuit is removed (safe restart mode).

The short winding protection will also protect in case of a secondary diode short-circuit.

OverTemperature Protection (OTP)

An accurate temperature protection is provided in the circuit. When the junction temperature exceeds the thermal shutdown temperature, the IC will enter the safe restart mode.

When the V_{start} level is reached, switching starts again. This process is repeated as long as the OTP condition exists.

Control pin protection

If pin CTRL is open-circuit or not connected, a fault condition is assumed and the converter will stop switching. Operation will recommence as soon as the fault condition is removed.

Soft start-up

To prevent transformer rattle during hiccup, the transformer peak current is slowly increased by the soft start function. This can be achieved by inserting a resistor and a capacitor between pin I_{sense} and the sense resistor (see Fig.11). An internal current source charges the capacitor to $V = I_{SS} \times R_{SS}$, with a maximum of approximately 0.5 V.

The start level and the time constant of the increasing primary current level can be adjusted externally by changing the values of R_{SS} and C_{SS}.

$$I_{primary(max)} = \frac{V_{ocp} - (I_{SS} \times R_{SS})}{R_{sense}}$$

$$\tau = R_{SS} \times C_{SS}$$

The charging current I_{SS} will flow as long as the voltage on pin I_{sense} is below approximately 0.5 V. If the voltage on pin I_{sense} exceeds 0.5 V, the soft start current source will start limiting the current I_{SS}. At the $V_{CC(start)}$ level, the I_{SS} current source is completely switched off.

Since the soft start current I_{SS} is supplied from pin DRAIN, the R_{SS} value will not affect the V_{CC} current during start-up.

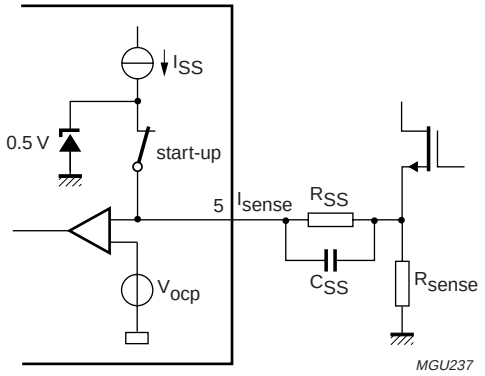


Fig.11 Soft start.

Driver

The driver circuit to the gate of the power MOSFET has a current sourcing capability of 135 mA typical and a current sink capability of 560 mA typical. This permits fast turn-on and turn-off of the power MOSFET for efficient operation.

A low driver source current has been chosen to limit the $\Delta V/\Delta t$ at switch-on. This reduces Electro Magnetic Interference (EMI) and also limits the current spikes across R_{sense}.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Voltages					
V_{CC}	supply voltage	continuous	–0.4	+20	V
V_{CTRL}	voltage on pin CTRL		–0.4	+5	V
V_{DEM}	voltage on pin DEM	current limited	–0.4	–	V
V_{sense}	voltage on pin I_{sense}	current limited	–0.4	–	V
V_{DRAIN}	voltage on pin DRAIN		–0.4	+650	V
Currents					
I_{CTRL}	current on pin CTRL		–	5	mA
I_{DEM}	current on pin DEM		–250	+250	μA
I_{sense}	current on pin I_{sense}		–1	+10	mA
I_{DRIVER}	current on pin DRIVER	d < 10 %	–0.8	+2	A
I_{DRAIN}	current on pin DRAIN		–	5	mA
General					
P_{tot}	total power dissipation	T_{amb} < 70 °C	–	0.75	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–20	+145	°C
V_{esd}	electrostatic discharge voltage				
	all pins except pins DRAIN and V_{CC}	HBM class 1; note 2	–	2000	V
	pins DRAIN and V_{CC}	HBM class 1; note 2	–	1500	V
	any pin	MM; note 3	–	400	V

Notes

1. All voltages are measured with respect to ground; positive currents flow into the IC; pin V_{CC} may not be current driven. The voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the maximum power rating is not violated.
2. Human Body Model (HBM): equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
3. Machine Model (MM): equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	100	K/W

QUALITY SPECIFICATION

In accordance with *'SNW-FQ-611-D'*.

CHARACTERISTICS

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Start-up current source (pin DRAIN)						
I_{DRAIN}	supply current drawn from pin DRAIN	$V_{CC} < V_{start}$	–	500	–	µA
		$V_{CC} > V_{start}$	–	50	–	µA
BV_{DSS}	breakdown voltage		650	–	–	V
Supply voltage management (pin V_{CC})						
$V_{CC(start)}$	start-up voltage on V_{CC}		10.3	11	11.7	V
$V_{CC(UVLO)}$	undervoltage lock-out on V_{CC}		8.1	8.7	9.3	V
$V_{CC(hys)}$	hysteresis voltage on V_{CC}	$V_{CC(start)} - V_{CC(UVLO)}$	2.0	2.3	2.6	V
$I_{CC(oper)}$	supply current under normal operation	no load on pin DRIVER	1.1	1.3	1.5	mA
$I_{CC(start)}$	supply current in start-up and safe restart mode	$V_{CC} < V_{start}$	0[1]	–	70	µA
$I_{CC(protection)}$	supply current while not switching	$V_{CC} > V_{UVLO}$	–	0.85	–	mA
Demagnetization management (pin DEM)						
$V_{th(DEM)}$	demagnetization comparator threshold voltage on pin DEM		50	100	150	mV
$I_{prot(DEM)}$	protection current on pin DEM	V_{DEM} = 50 mV	–50[2]	–	–10	nA
$V_{clamp(DEM)(neg)}$	negative clamp voltage on pin DEM	I_{DEM} = –150 µA	–0.5	–0.25	–0.05	V
$V_{clamp(DEM)(pos)}$	positive clamp voltage on pin DEM	I_{DEM} = 250 µA	0.5	0.7	0.9	V
t_{suppr}	suppression of transformer ringing at start of secondary stroke		1.1	1.5	1.9	µs
Pulse width modulator						
$t_{on(min)}$	minimum on-time		–	t_{leb}	–	ns
$t_{on(max)}$	maximum on-time	latched	40	50	60	µs
Oscillator						
$f_{osc(l)}$	oscillator low fixed frequency	V_{CTRL} > 1.5 V	20	25	30	kHz
$f_{osc(h)}$	oscillator high fixed frequency	V_{CTRL} < 1 V	145	175	205	kHz
$V_{vco(start)}$	peak voltage on pin I_{sense}; where frequency reduction starts	see Figs 7 and 8	–	VCO_1	–	mV
$V_{vco(nom)}$	peak voltage on pin I_{sense}; where the frequency is equal to $f_{osc(l)}$		–	VCO_1 – 50	–	mV
Duty cycle control (pin CTRL)						
$V_{CTRL(min)}$	minimum voltage on pin CTRL for maximum duty cycle		–	1.0	–	V
$V_{CTRL(max)}$	maximum voltage on pin CTRL for minimum duty cycle		–	1.5	–	V
$I_{prot(CTRL)}$	protection current on pin CTRL	V_{CTRL} = 1.5 V	–1[2]	–0.8	–0.5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Valley switch (pin DRAIN)						
$\Delta V/\Delta t_{valley}$	valley recognition voltage change		−85	–	+85	V/µs
$t_{valley-swon}$	delay from valley recognition to switch-on		–	150(2)	–	ns
Overcurrent and short winding protection (pin I_{sense})						
$V_{sense(max)}$	maximum source voltage OCP	$\Delta V/\Delta t$ = 0.1 V/µs	0.48	0.52	0.56	V
t_{PD}	propagating delay from detecting $V_{sense(max)}$ to switch-off	$\Delta V/\Delta t$ = 0.5 V/µs	–	140	185	ns
V_{swp}	short winding protection voltage		0.83	0.88	0.96	V
t_{leb}	blanking time for current and short winding protection		300	370	440	ns
I_{SS}	soft start current	V_{sense} < 0.5 V	45	60	75	µA
Overvoltage protection (pin DEM)						
$I_{OVP(DEM)}$	OVP level on pin DEM	set by resistor R_{DEM}; see Section “OverVoltage Protection (OVP)”	54	60	66	µA
Overpower protection (pin DEM)						
$I_{OPP(DEM)}$	OPP current on pin DEM to start OPP correction	set by resistor R_{DEM}; see Section “OverPower Protection (OPP)”	–	−24	–	µA
$I_{OPP50\%(DEM)}$	OPP current on pin DEM; where maximum source voltage is limited to 0.3 V		–	−100	–	µA
Driver (pin DRIVER)						
I_{source}	source current capability of driver	V_{CC} = 9.5 V; V_{DRIVER} = 2 V	–	−135	–	mA
I_{sink}	sink current capability of driver	V_{CC}= 9.5 V; V_{DRIVER} = 2 V	–	240	–	mA
		V_{CC} = 9.5 V; V_{DRIVER} = 9.5 V	–	560	–	mA
$V_{o(max)}$	maximum output voltage of the driver	V_{CC} > 12 V	–	11.5	12	V
Overtemperature protection						
$T_{prot(max)}$	maximum temperature protection level		130	140	150	°C
$T_{prot(hys)}$	hysteresis for the temperature protection level		–	8(2)	–	°C

Notes

1. For $V_{CC} \geq 2$ V.
2. Guaranteed by design.

APPLICATION INFORMATION

A converter with the TEA1506 consists of an input filter, a transformer with a third winding (auxiliary), and an output stage with a feedback circuit.

Capacitor C_{VCC} (at pin V_{CC}) buffers the supply voltage of the IC, which is powered via the resistor R_S during start-up and via the auxiliary winding during operation.

A sense resistor converts the primary current into a voltage at pin I_{sense}. The value of this sense resistor defines the maximum primary peak current.

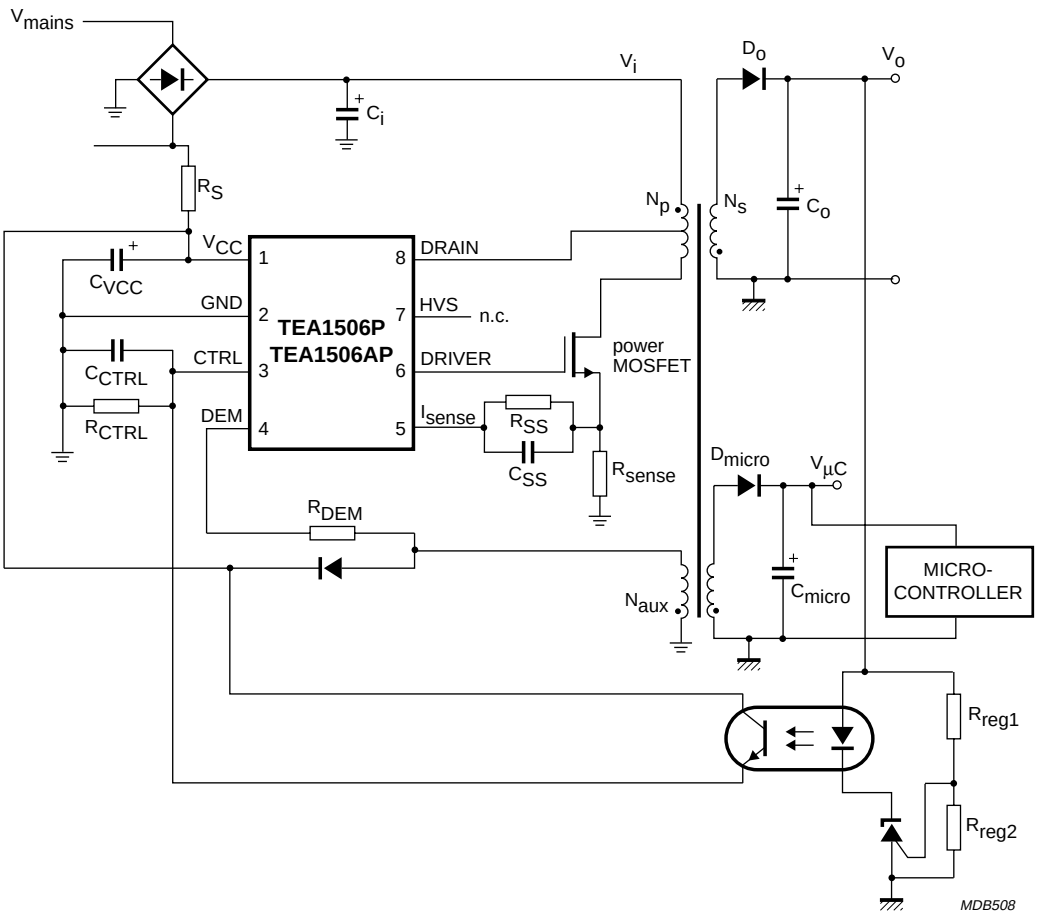


Fig.12 Flyback configuration with secondary sensing.

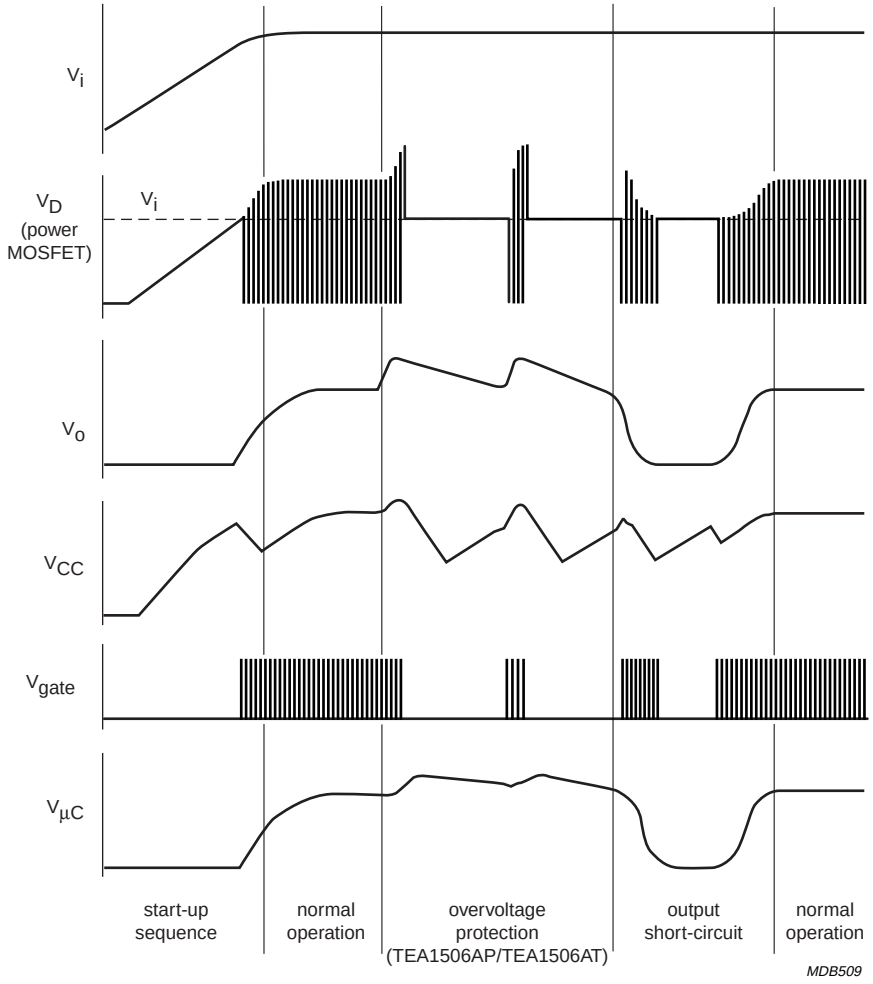
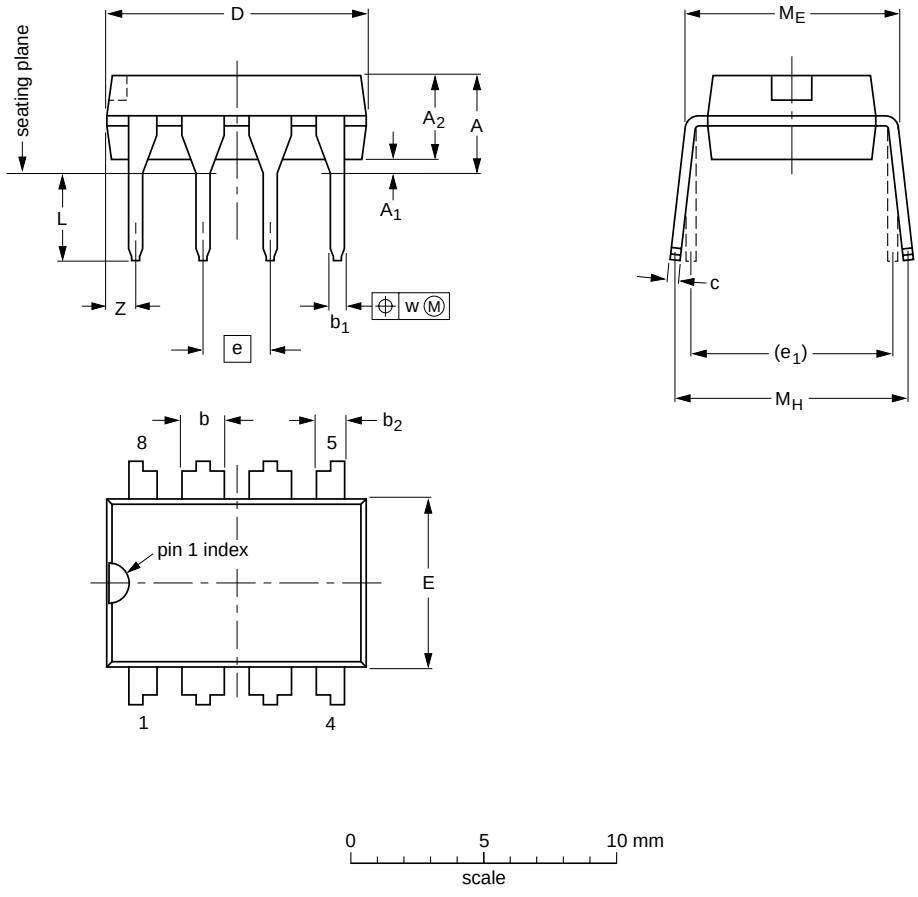


Fig.13 Typical waveforms.

PACKAGE OUTLINES

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

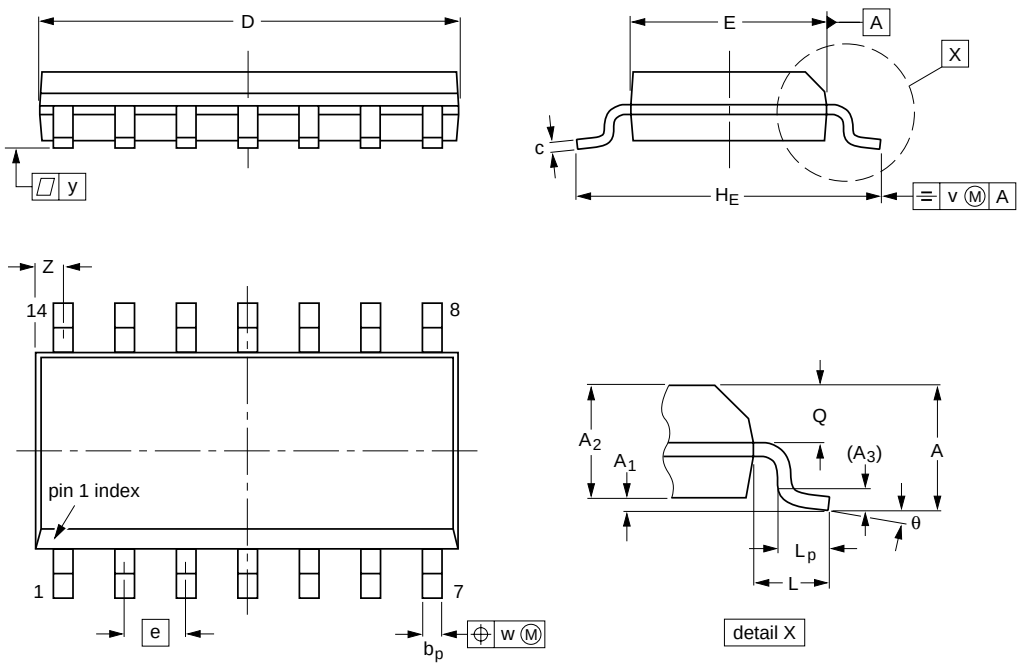
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.02	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT97-1	050G01	MO-001	SC-504-8			~~99-12-27~~ 03-02-13

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all the BGA and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe

dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE(1)	SOLDERING METHOD		
		WAVE	REFLOW(2)	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable(3)	–	suitable
Through-hole-surface mount	PMFP(9)	not suitable	not suitable	–
Surface mount	BGA, LBGA, LFBGA, SQFP, SSOP-T(4), TFBGA, VFBGA	not suitable	suitable	–
	DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable(5)	suitable	–
	PLCC(6), SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended(6)(7)	suitable	–
	SSOP, TSSOP, VSO, VSSOP	not recommended(8)	suitable	–

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
4. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
5. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
6. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
7. Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
8. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
9. Hot bar soldering or manual soldering is suitable for PMFP packages.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
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Notes

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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